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FIG. 1a

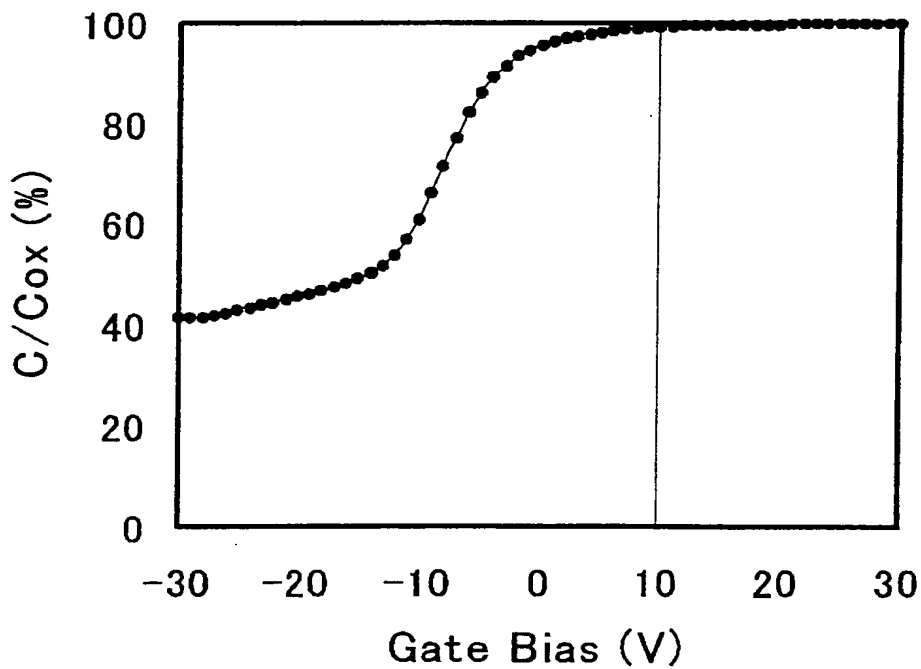
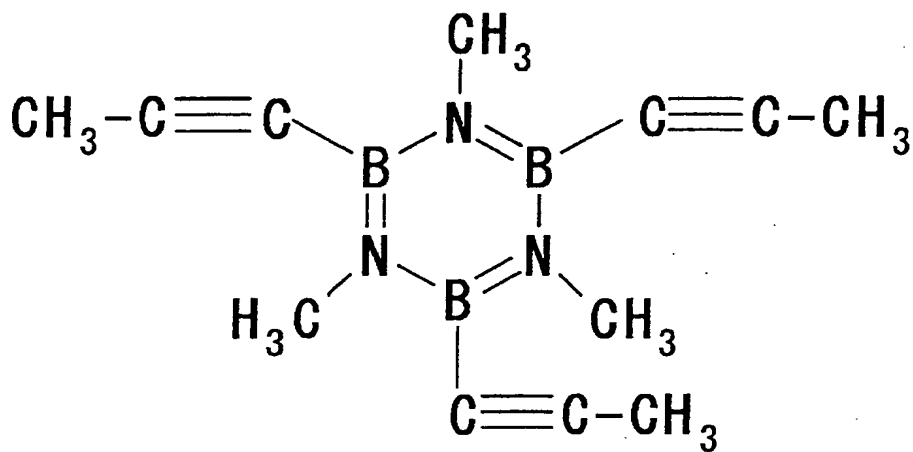


FIG. 1b

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FIG. 2a

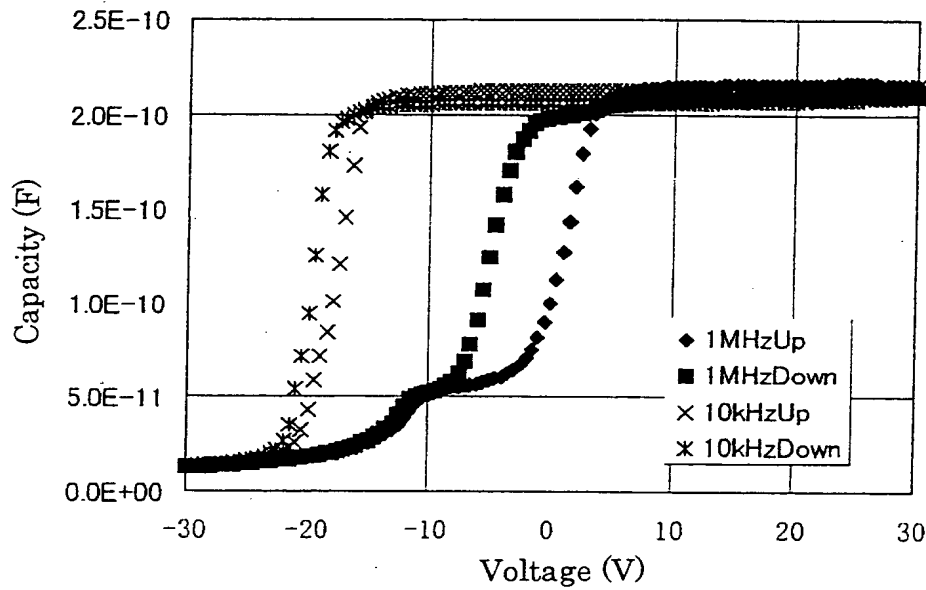
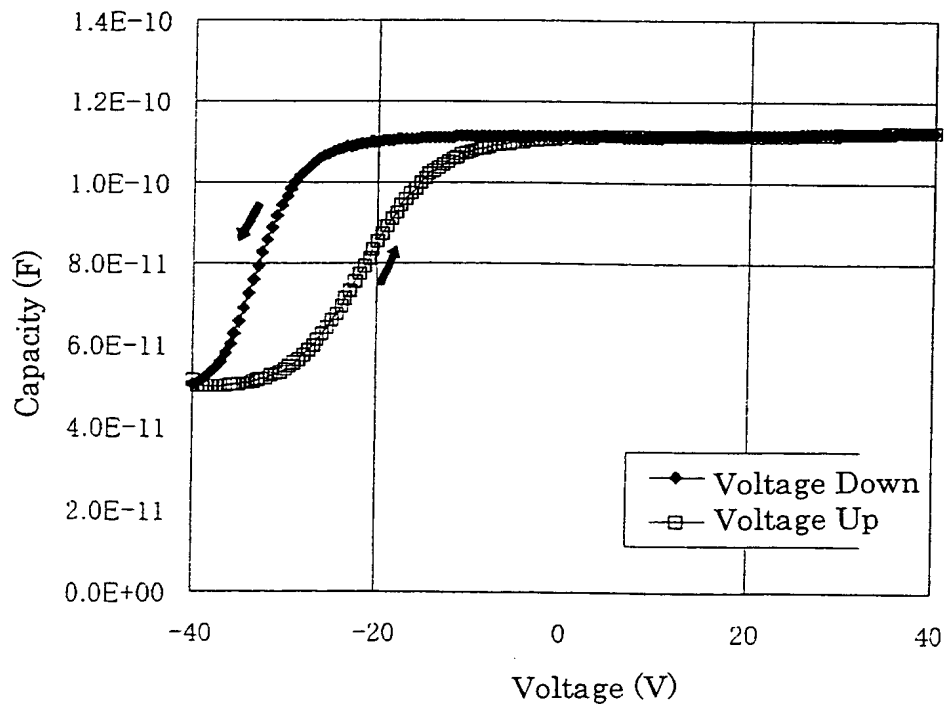


FIG. 2b



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FIG. 3a

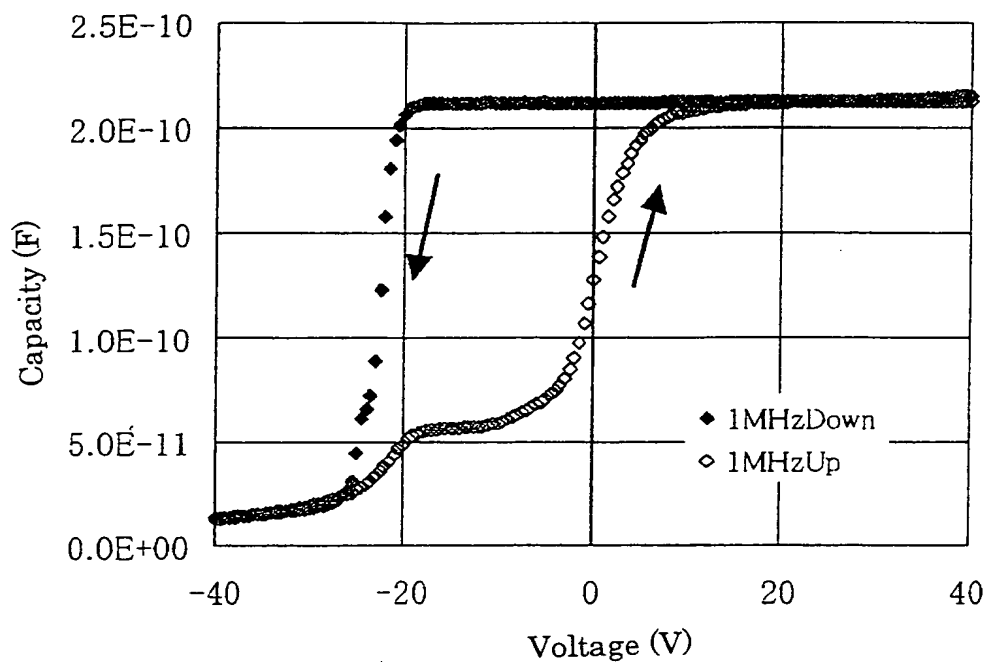


FIG. 3b

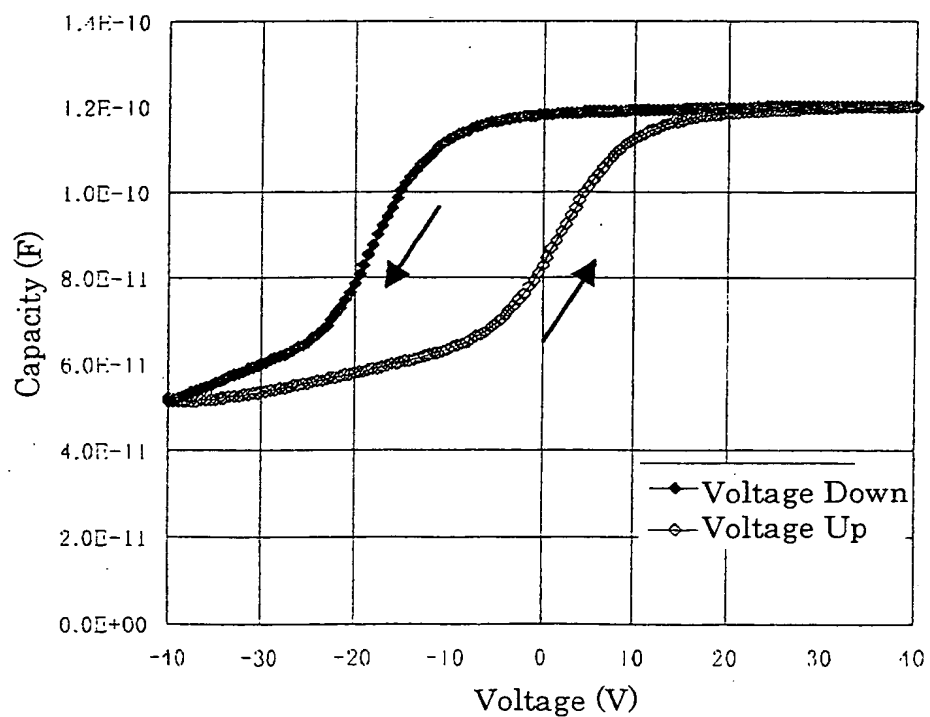


FIG. 4a

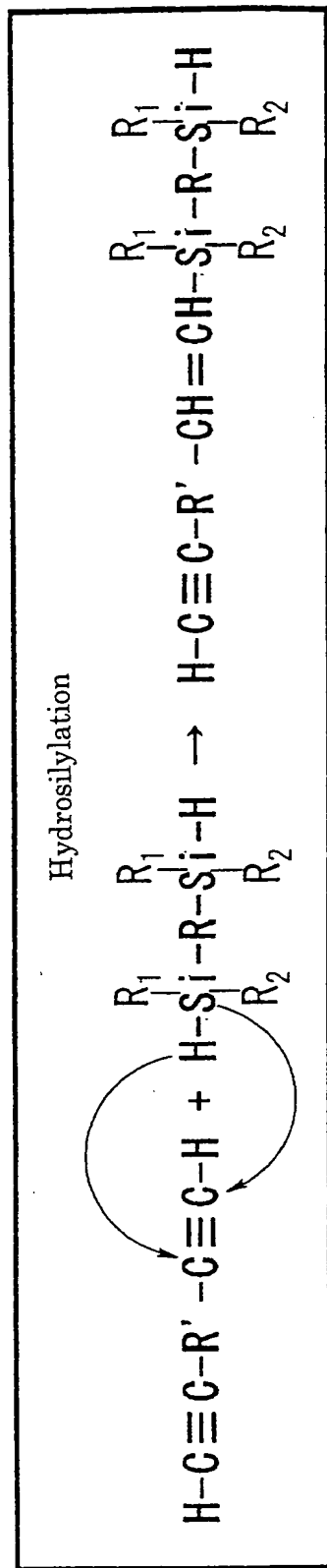


FIG. 4b

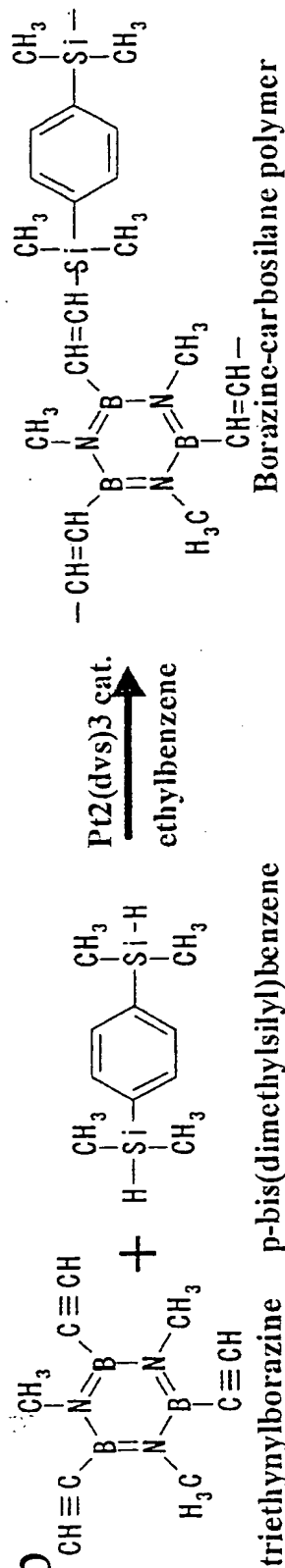
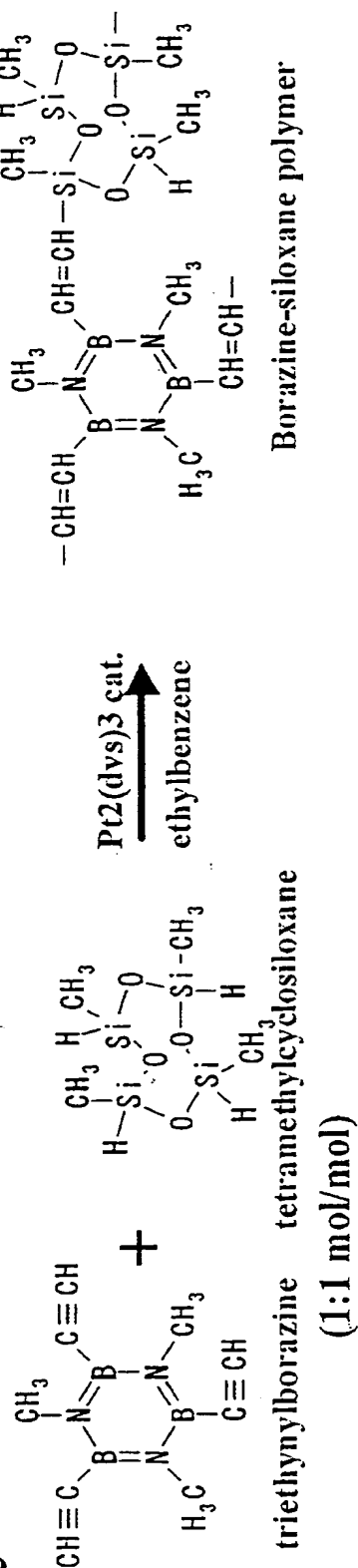
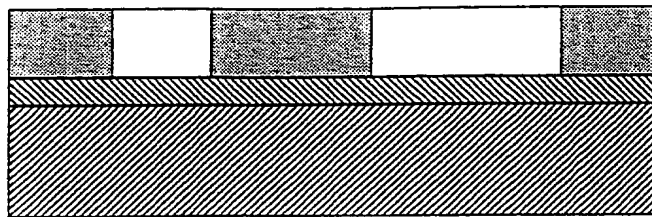


FIG. 4c



Attachment of metal mask to sample



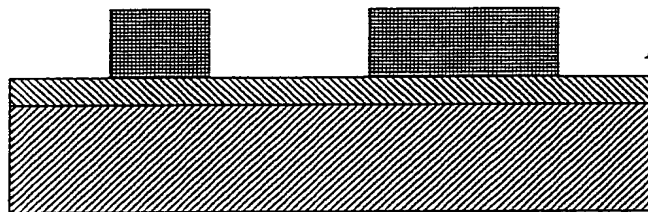
Metal mask

Borazine polymer

Silicon substrate

FIG. 5a

Removal of mask after evaporation of aluminum



Aluminum electrode

FIG. 5b

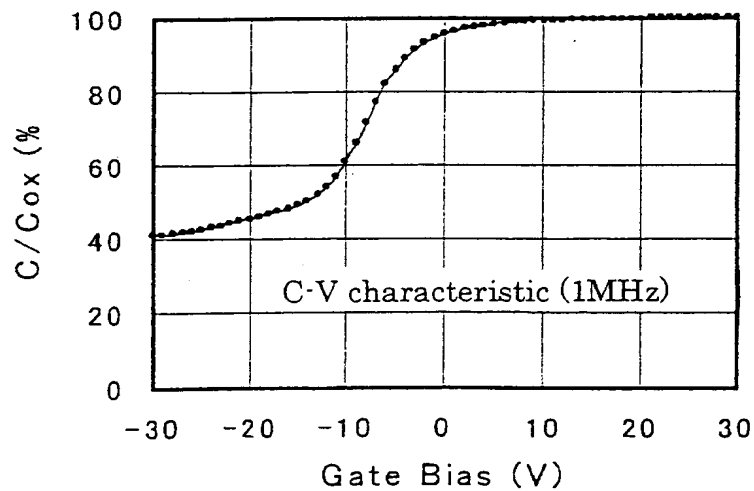
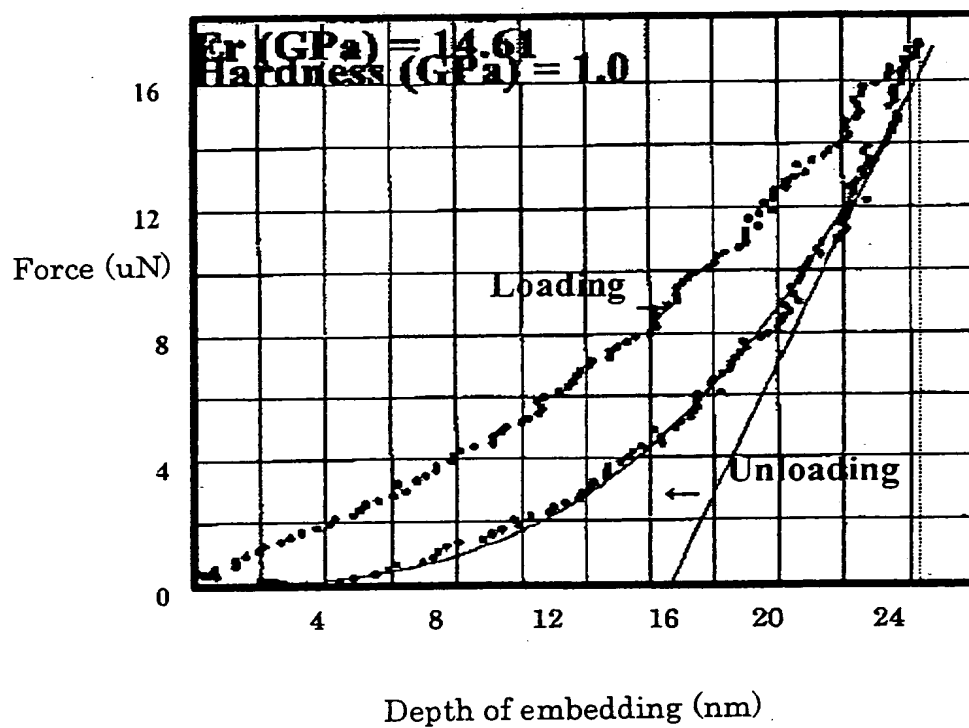


FIG. 5c

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FIG. 6



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FIG. 7a

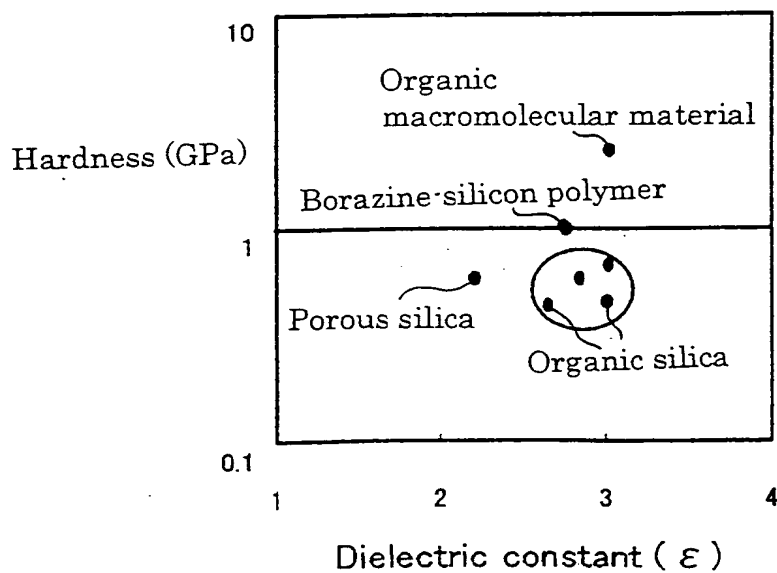
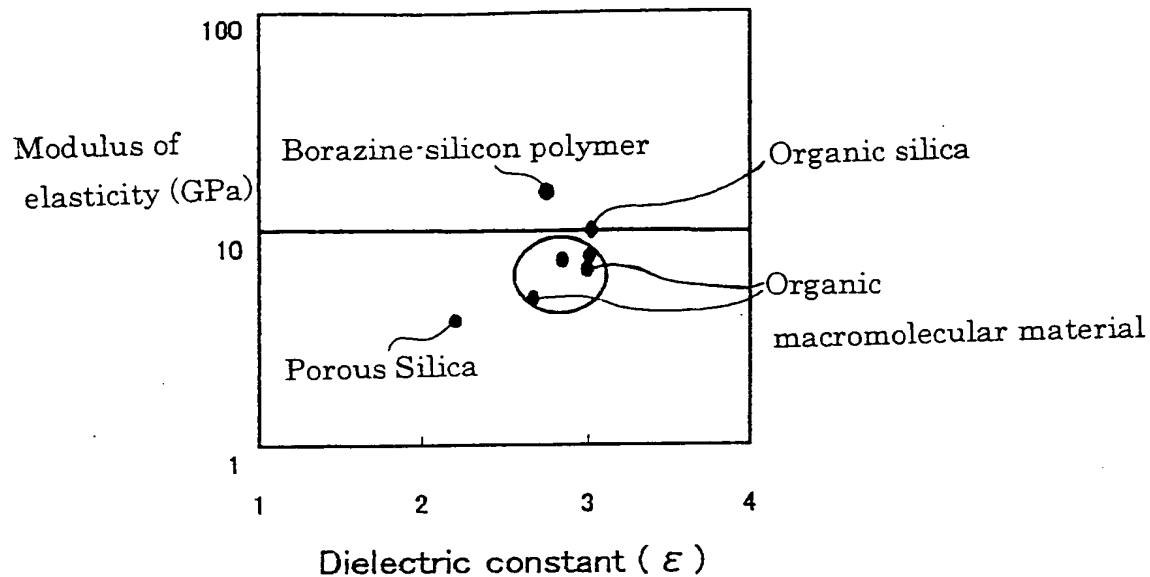
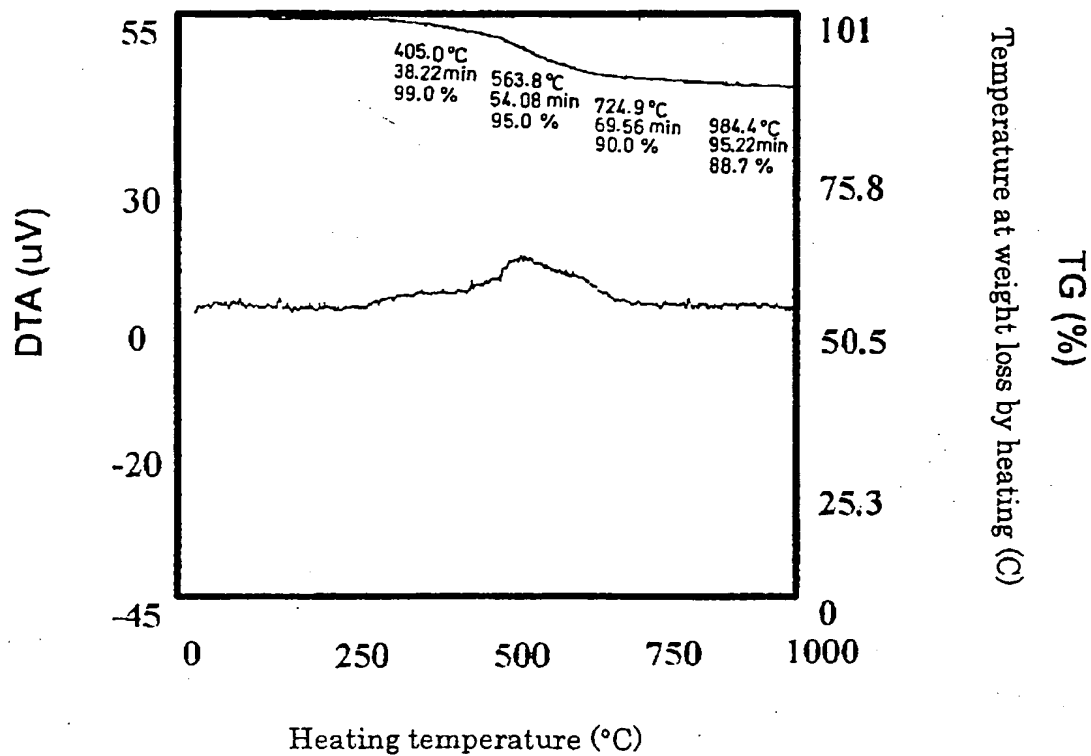


FIG. 7b

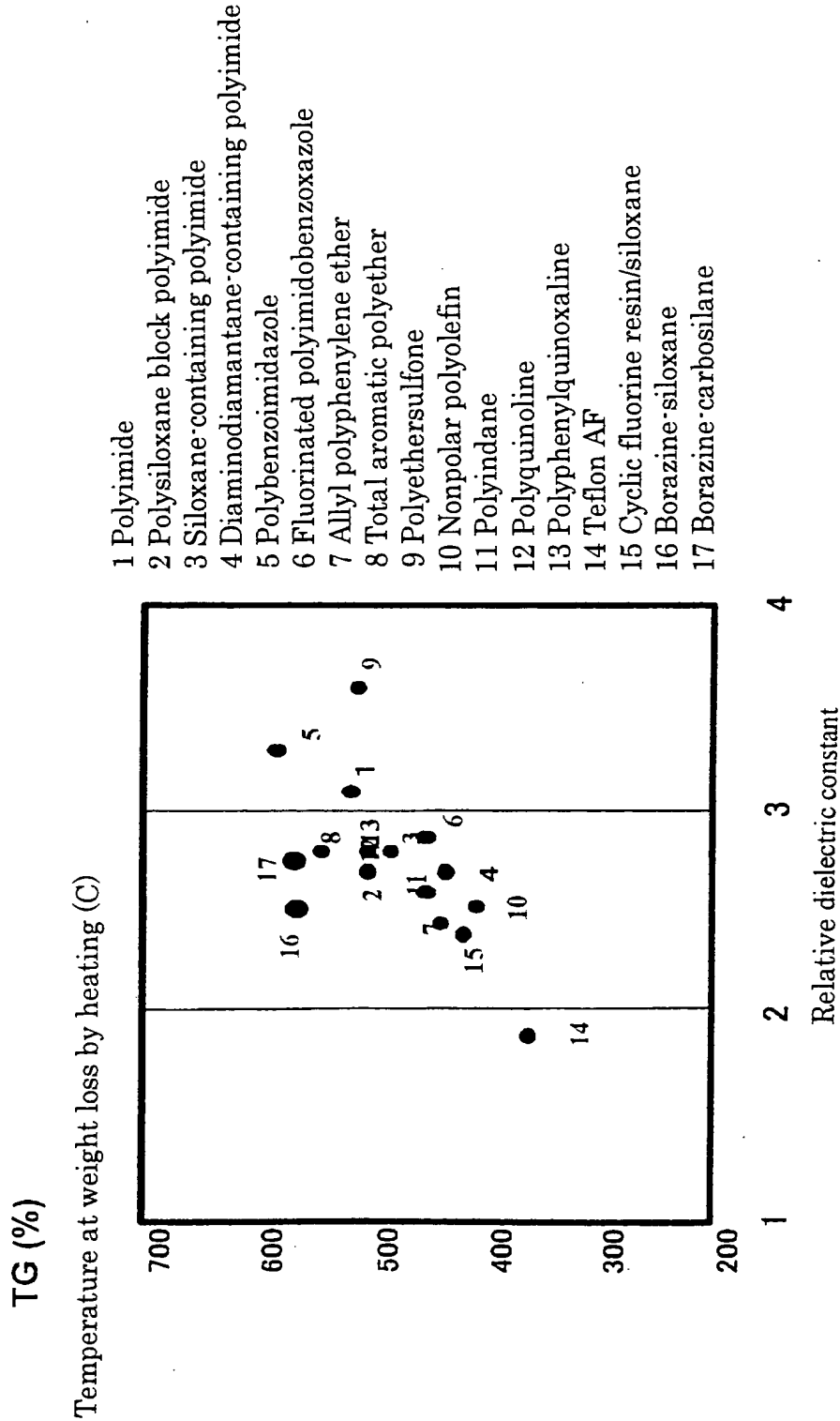
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FIG. 8



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FIG. 9



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FIG. 10

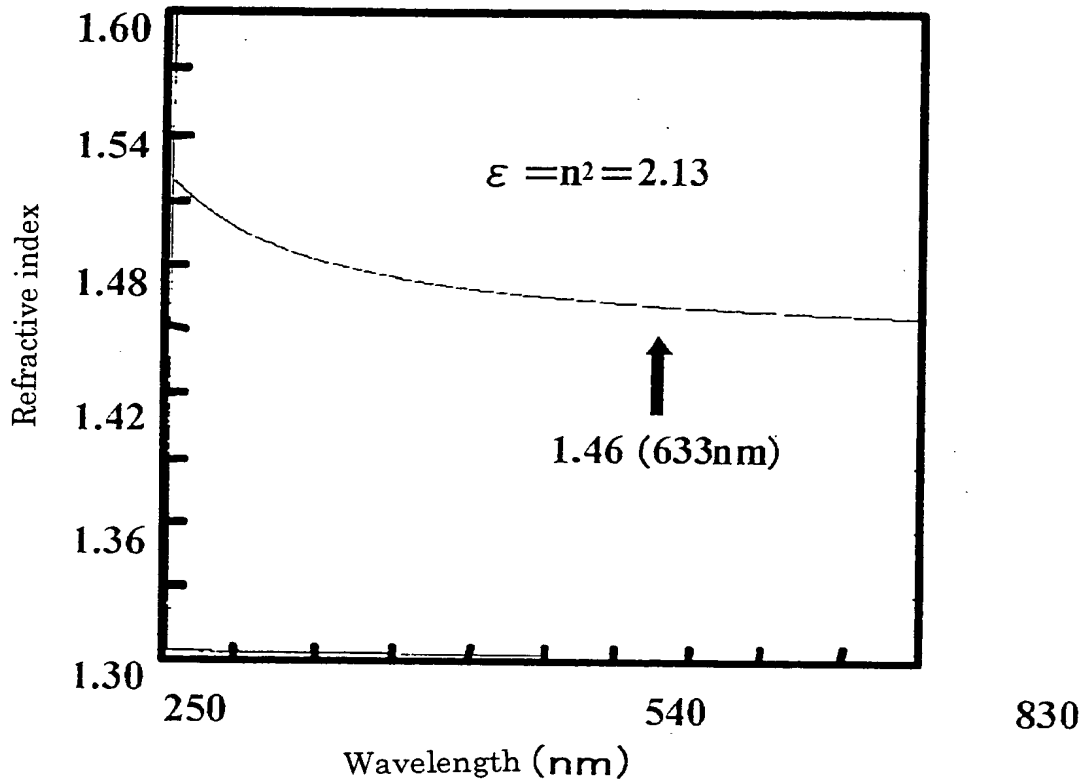
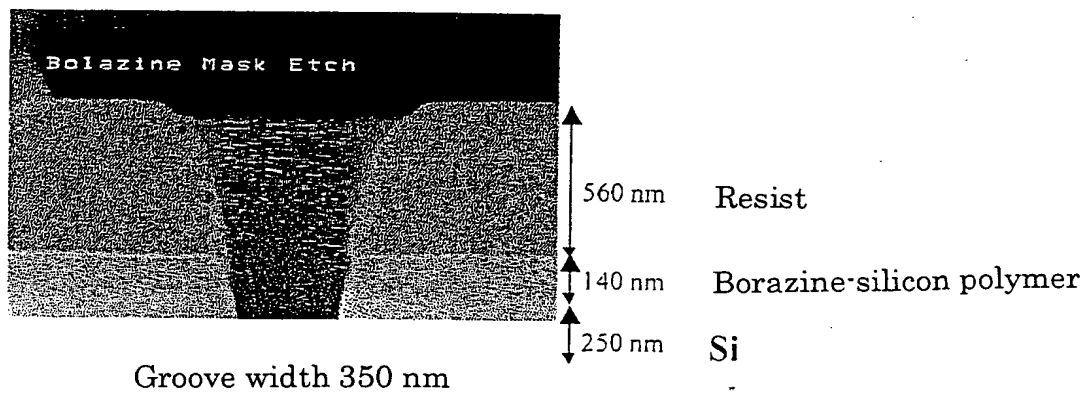


FIG. 11



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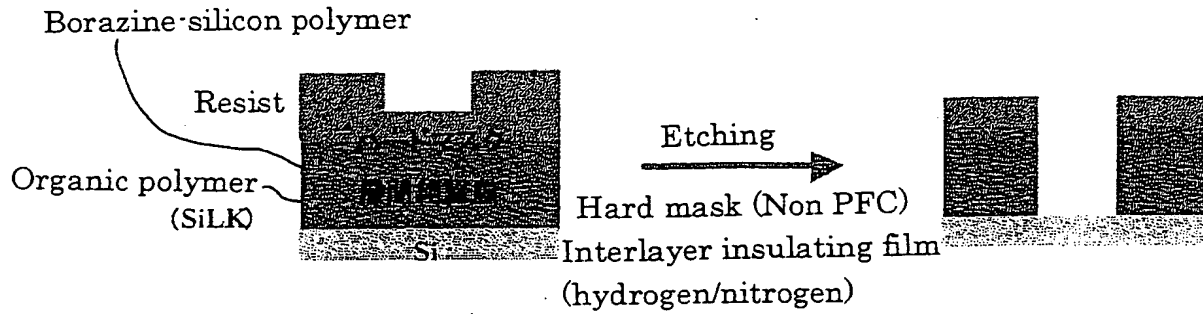


FIG. 12a

FIG. 12b

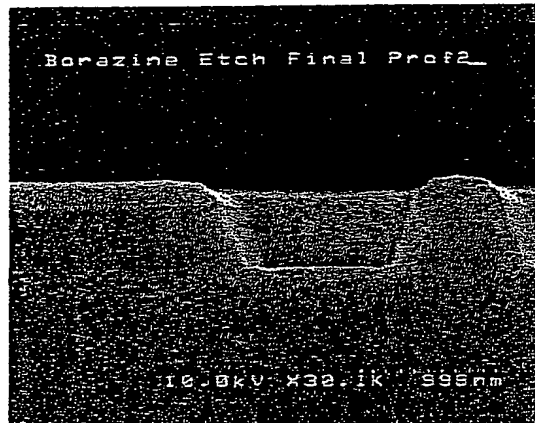


FIG. 12c

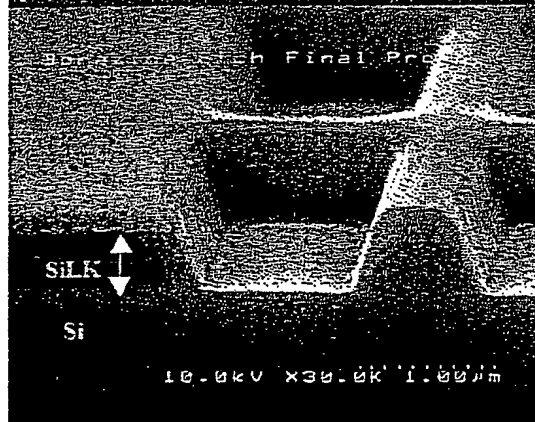


FIG. 12d

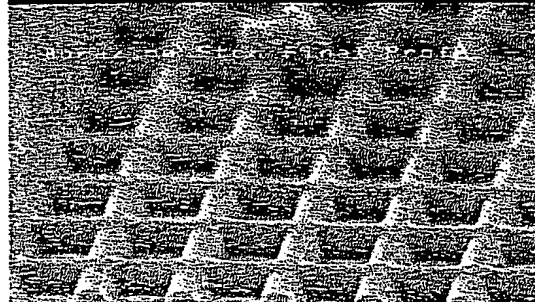


FIG. 13i

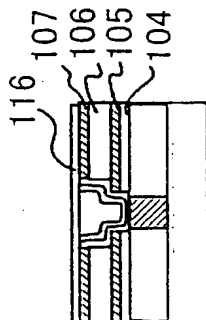


FIG. 13j

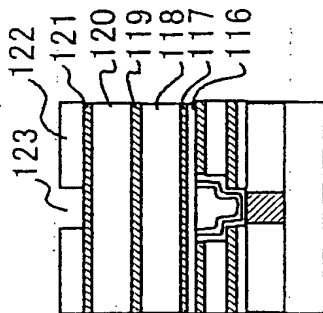


FIG. 13k

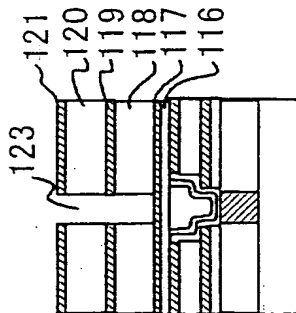


FIG. 13l

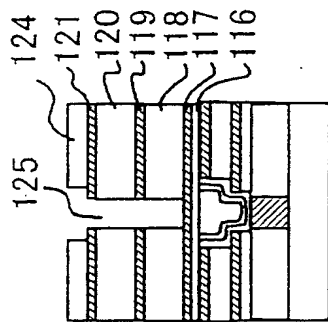


FIG. 13m

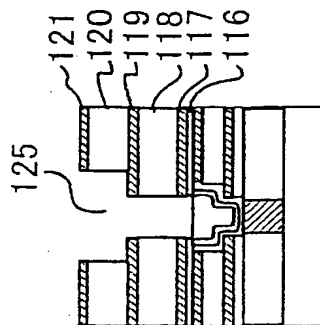


FIG. 13n

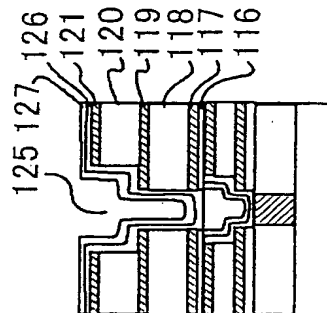


FIG. 13o

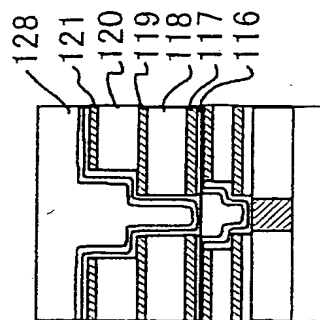
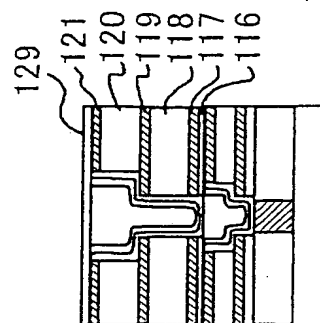
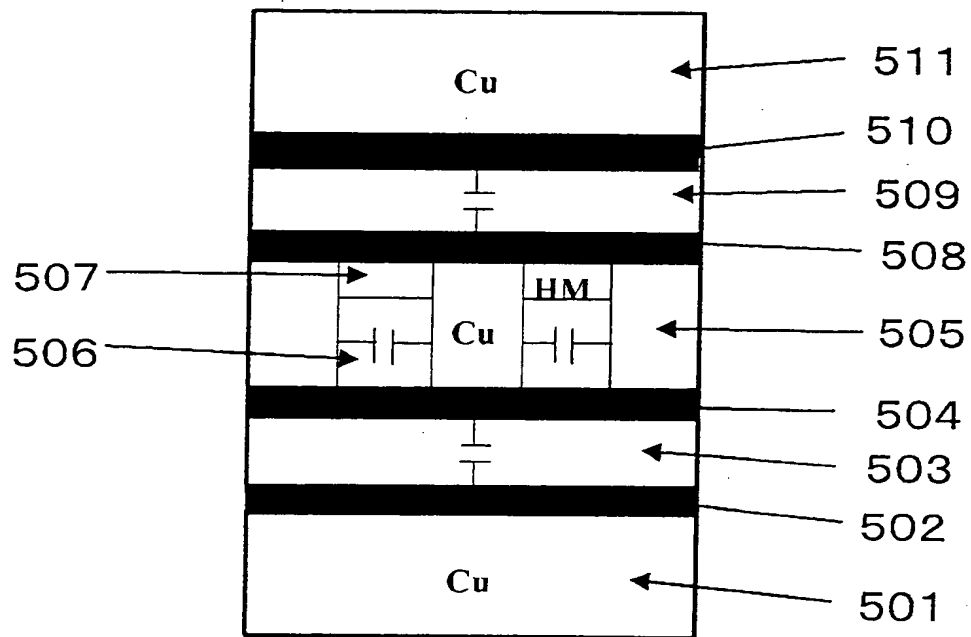


FIG. 13p



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FIG. 14



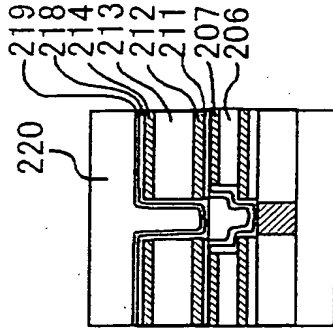


FIG. 15d

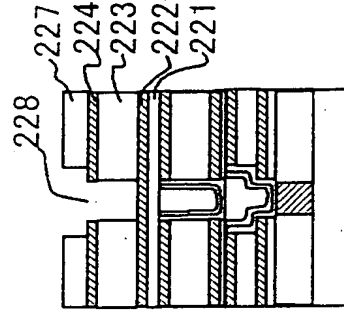


FIG. 15h

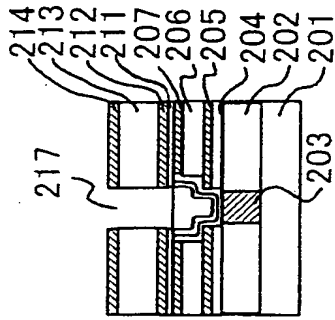


FIG. 15c

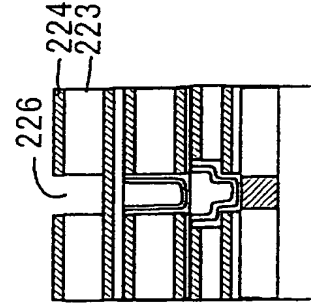


FIG. 15g

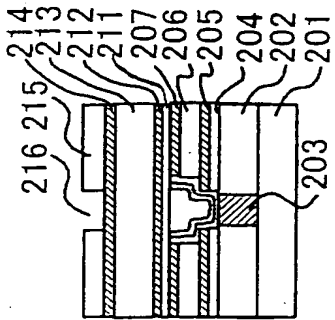


FIG. 15b

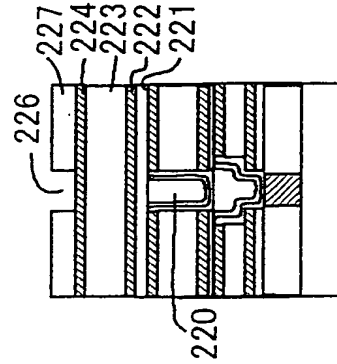


FIG. 15f

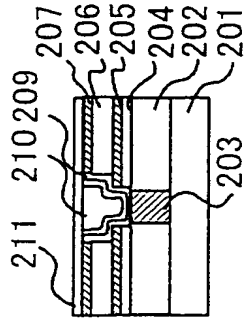


FIG. 15a

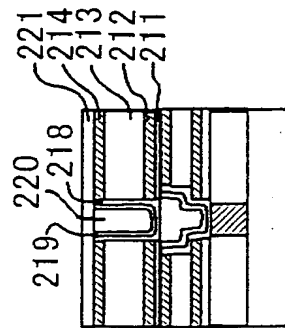


FIG. 15e

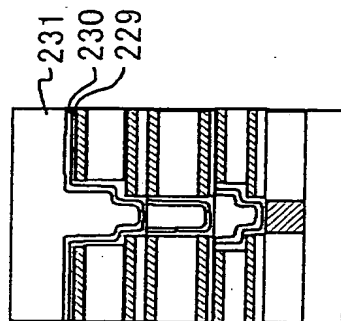


FIG. 15j

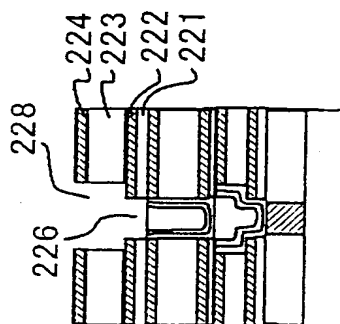


FIG. 15i

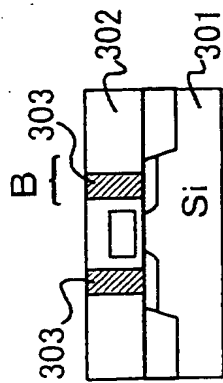


FIG. 16a

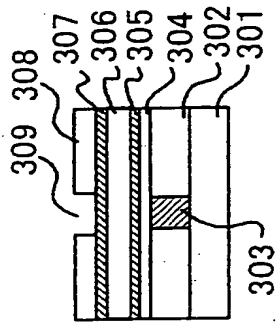


FIG. 16b

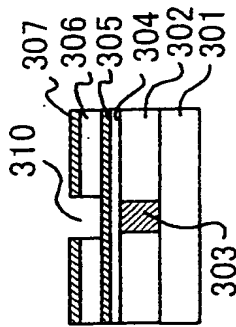


FIG. 16c

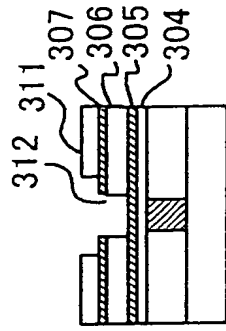


FIG. 16d

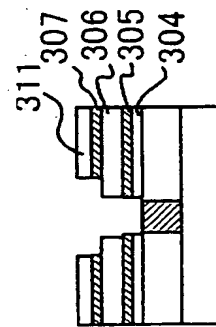


FIG. 16e

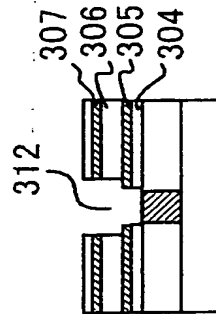


FIG. 16f

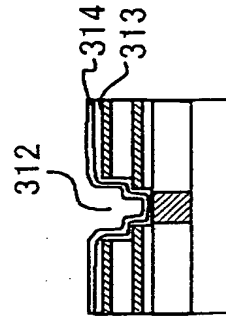


FIG. 16g

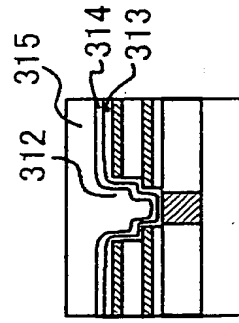


FIG. 16h

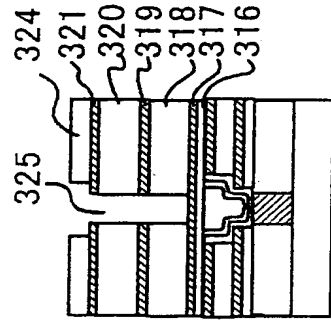


FIG. 16i

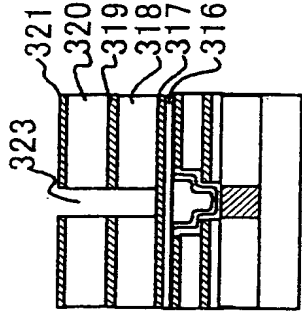


FIG. 16j

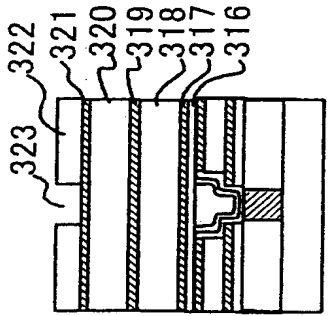


FIG. 16k

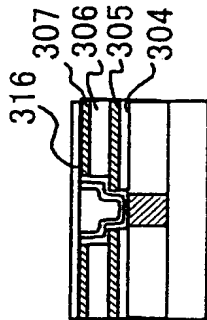


FIG. 16l

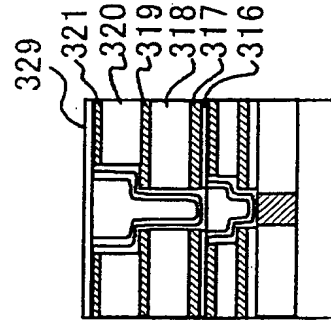


FIG. 16m

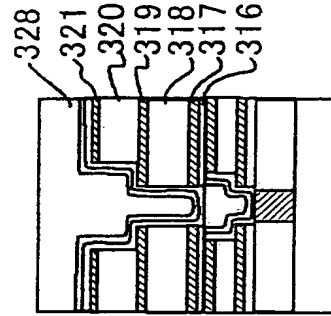


FIG. 16n

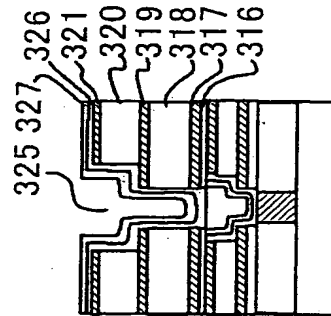


FIG. 16o

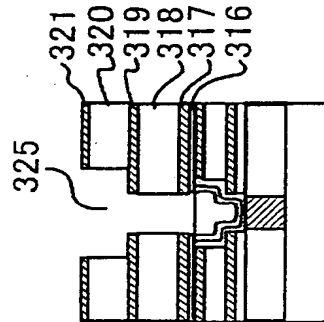


FIG. 16p

A cross-sectional view of a semiconductor device. The structure consists of a substrate with a series of layers. From bottom to top, the layers are: a white layer, a hatched layer, a white layer, a hatched layer, and a white layer. On top of the white layer, there is a small rectangular feature labeled 411. To the right of this feature, there are three more rectangular features labeled 404, 405, and 406, stacked vertically. A bracket labeled 410 spans the top of the 404, 405, and 406 features.

This diagram shows a cross-sectional view of a semiconductor device. It features a substrate with a trench. The trench is filled with a material, and the top surface of the trench is covered by a layer. Labels 402, 404, 405, and 406 point to different layers or regions, while label 411 points to the trench itself.

A cross-sectional view of a multi-layered structure. The structure consists of several layers. The top layer is labeled 415. Below it is a layer labeled 406. The bottom layer is labeled 405. The layers are separated by thin lines, and there are some internal features or gaps within the layers.

FIG. 17h

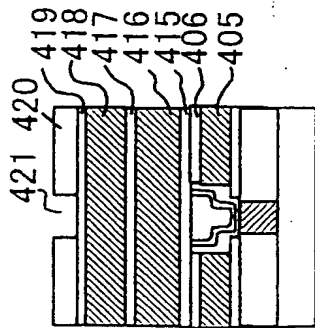


FIG. 17i

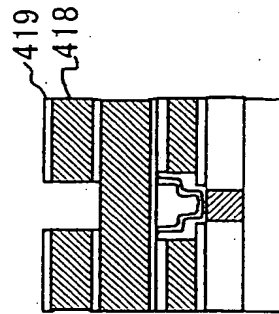


FIG. 17j

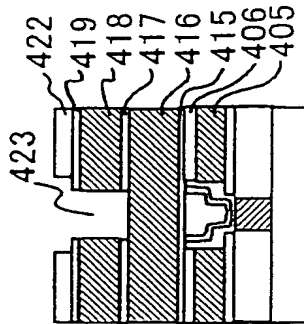


FIG. 17k

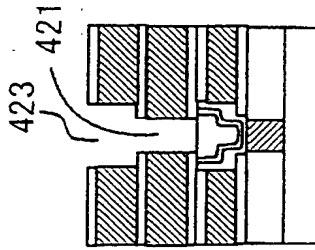


FIG. 17l

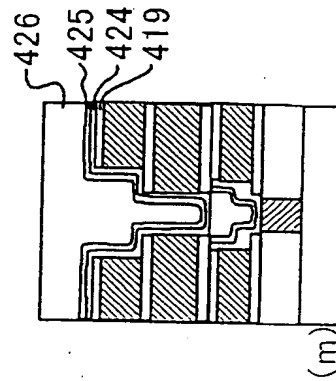


FIG. 17m

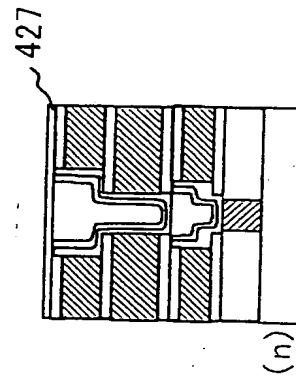
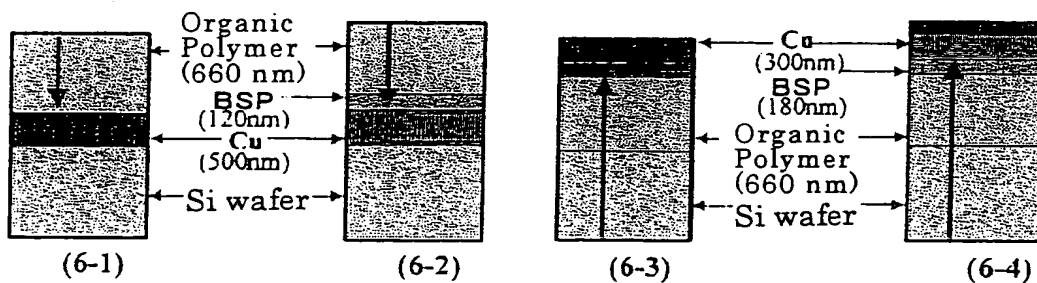


FIG. 17n

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FIG. 18a

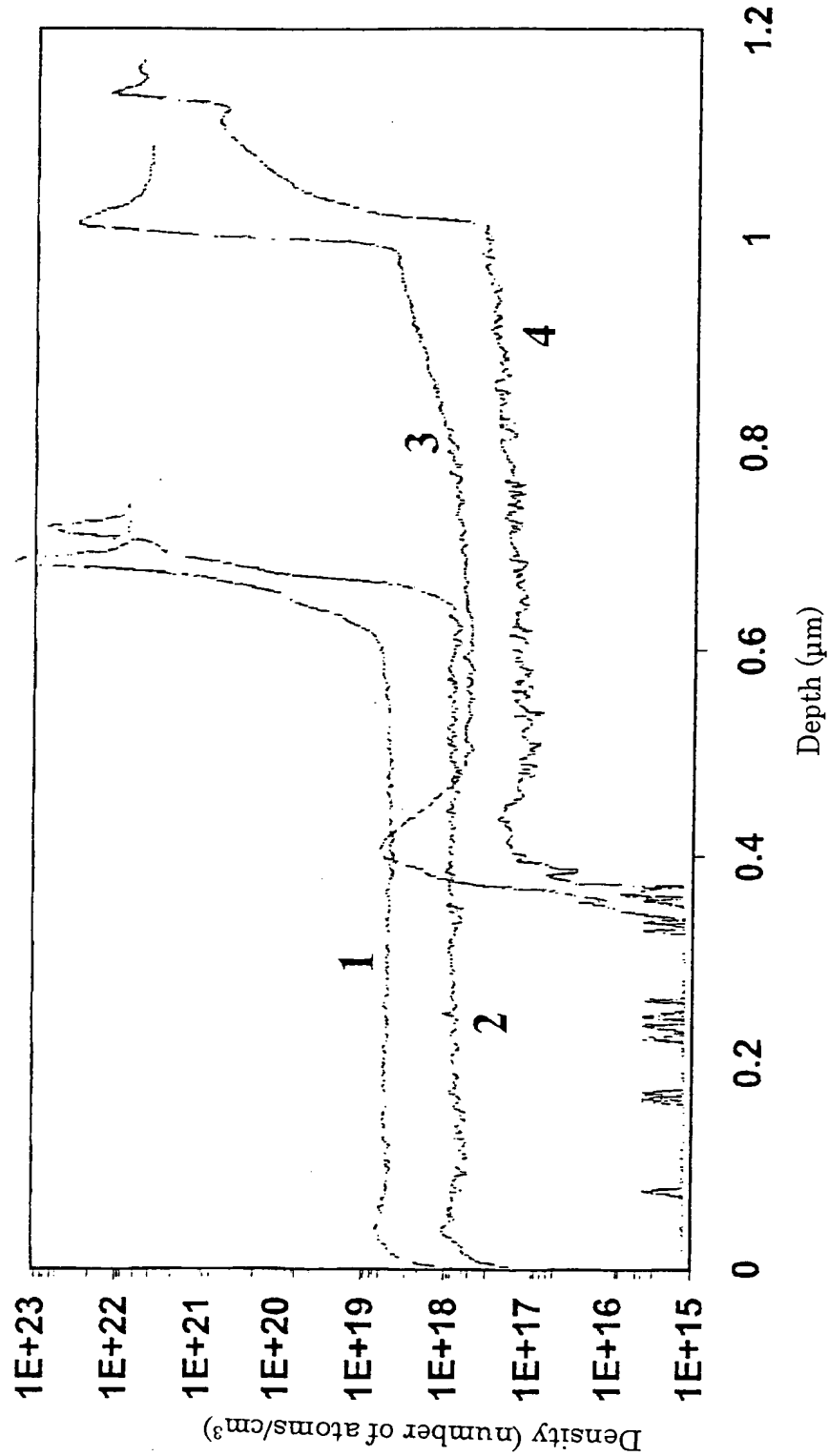


	Structure	Cu atoms/cm ³
1	Si / Cu(500nm) / OP(660nm)	5×10^{18}
2	Si / Cu(500nm) / BSP(120nm) / OP(660nm)	8×10^{17}
3	Si / OP(660nm) / Cu(300nm)	6×10^{17}
4	Si / OP(660nm) / BSP(180nm) / Cu(300nm)	1×10^{17}

FIG. 18b

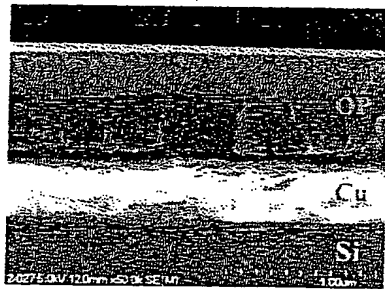
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FIG. 19



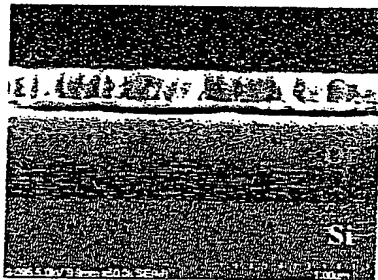
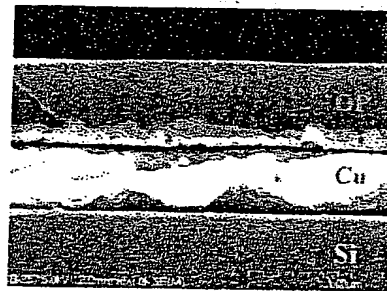
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FIG. 20a



Annealing
400°C
6hrs

FIG. 20b



Annealing
400°C
6hrs

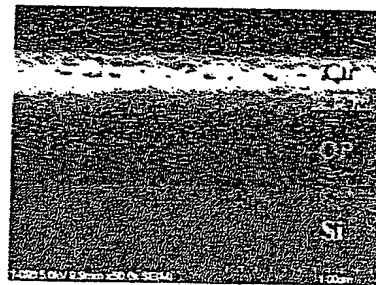


FIG. 20c

FIG. 20d

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FIG. 21a

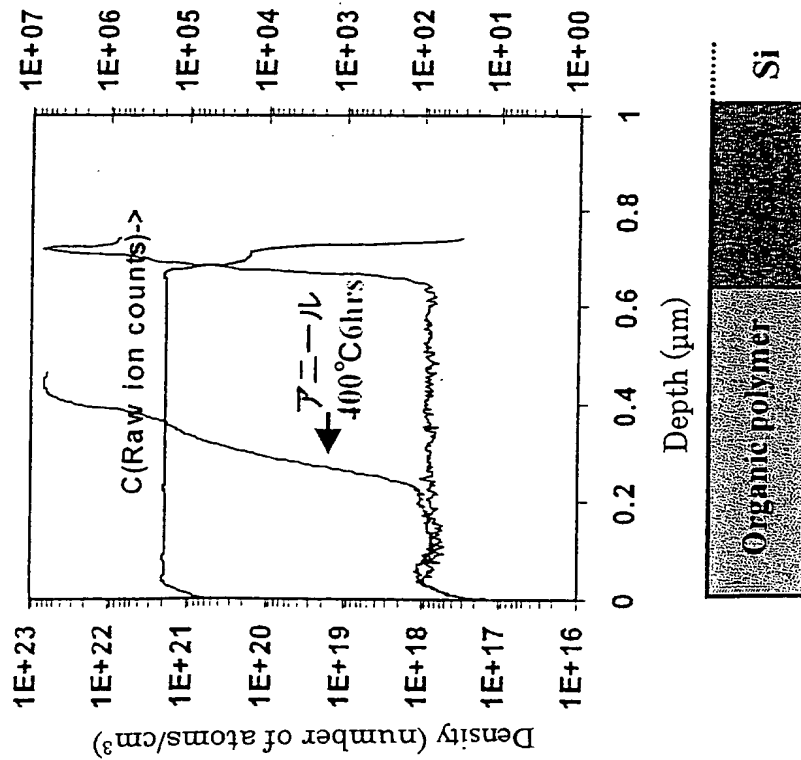


FIG. 21c

FIG. 21b

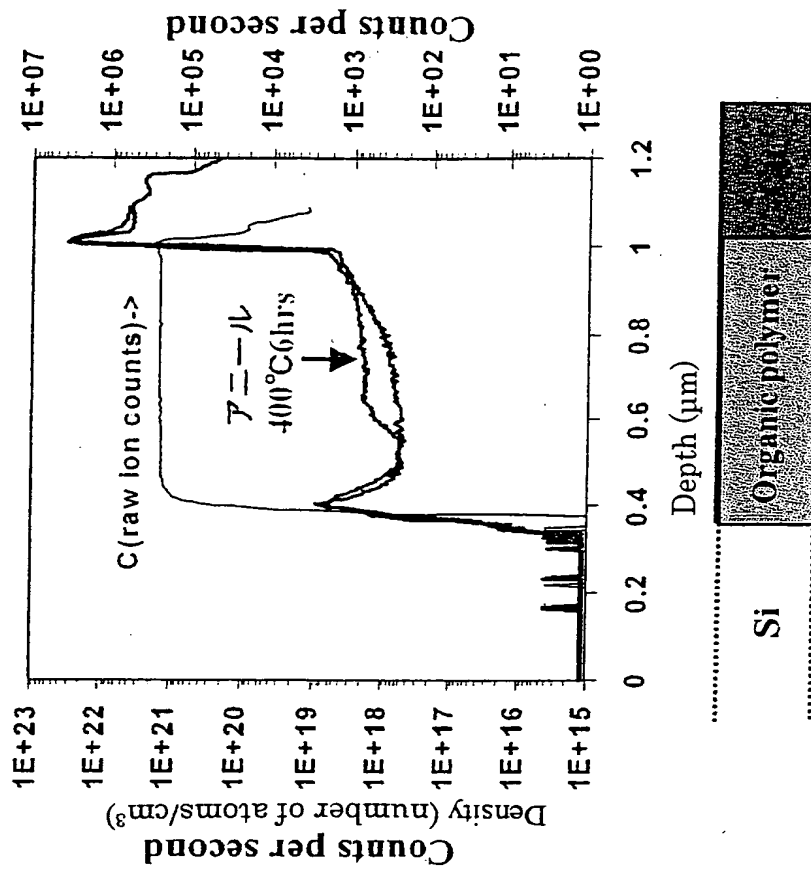
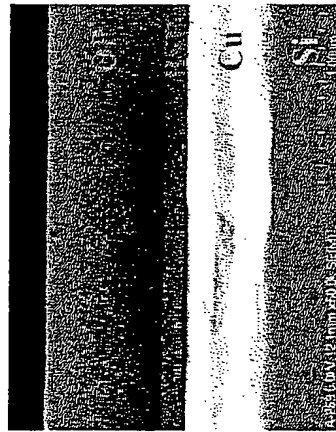


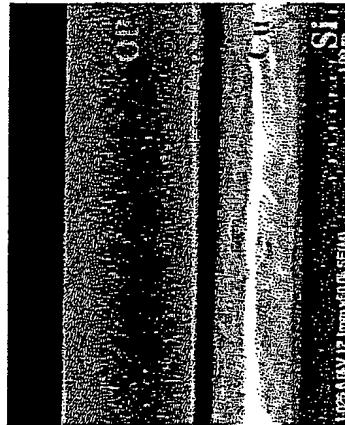
FIG. 21d

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FIG. 22



Annealing
↑
400°C·6hrs



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FIG. 23a

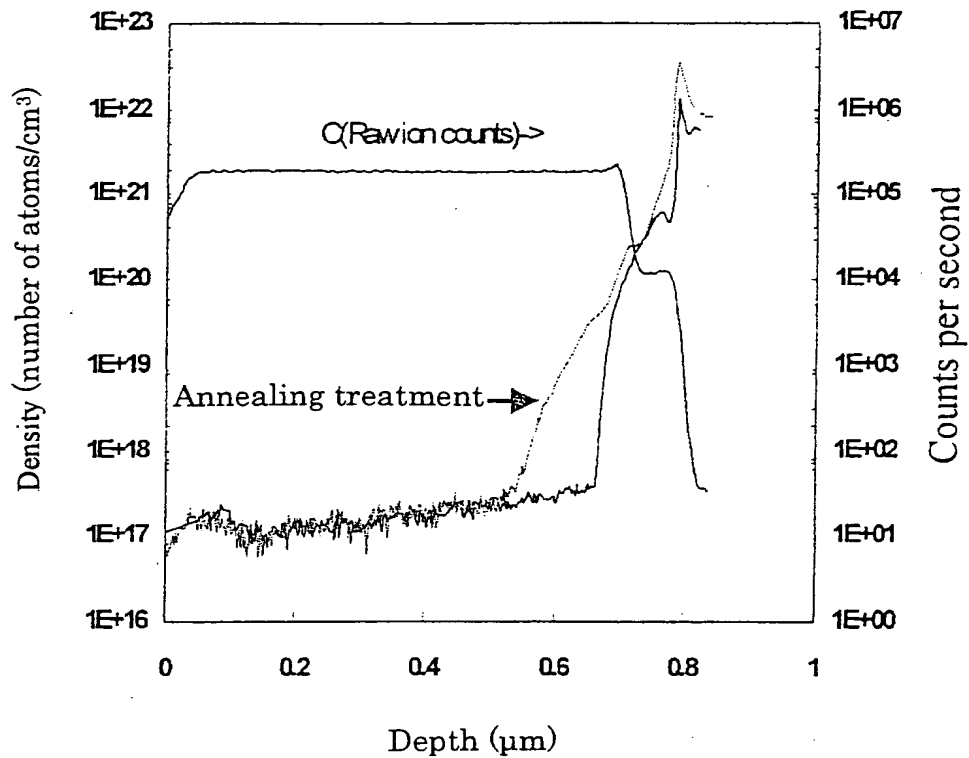
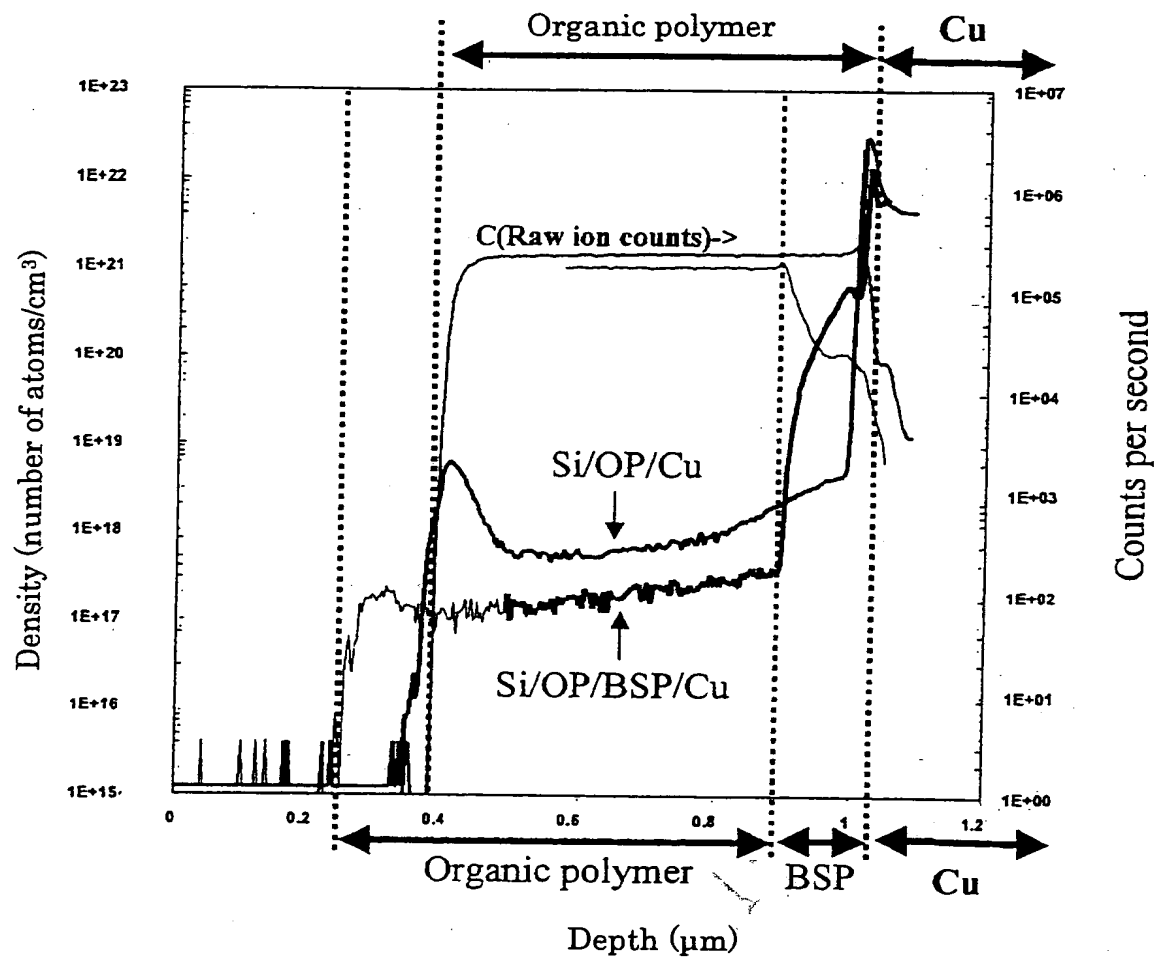


FIG. 23b

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FIG. 24



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